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[Amdmt. Transmittal]



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IN THE UNITED STATES PATENT  
AND TRADEMARK OFFICE

TECHNOLOGY CENTER 2800

Applicant: John M. Callahan

Docket No. NANO09DIV2

Serial No.: 10/014,928

Group Art Unit: 2814

Filed: December 11, 2001

Examiner: Ha, Nathan W.

For: DUAL DIE MEMORY

**Amendment and Response under Rule 121**

Assistant Commissioner for Patents  
U.S. Patent and Trademark Office  
P O Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated April 24, 2003, Applicant respectfully requests the Examiner to enter the following amendments to the claims and consider the following remarks under current Rule 121 amendment practice:

**IN THE CLAIMS:**

43. (Amended) A method of operating a dual-die, double-sized, back-to-back integrated-circuit chip assembly, comprising the steps of:

mounting a pair of integrated-circuit chips back-to-back, where each integrated-circuit chip has one or more pairs of reversible wire-bonding pads; and

electrically reversing internal connections to the wire-bonding-pads on one of the integrated-circuit chips so that pads on each integrated-circuit chip for similar functions are